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22879 7590 01/15/2010 HEWLETT-PACKARD COMPANY Intellectual Property Administration 3404 E. Harmony Road Mail Stop 35 FORT COLLINS, CO 80528			EXAMINER TANG, KENNETH	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary

Application No.

10/621,067

Applicant(s)

FARKAS ET AL.

Examiner

KENNETH TANG

Art Unit

2195

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 October 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,7,8,15,17-26 and 29-37 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,7,8,15,17-26 and 29-37 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB06)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

1. Claims 1-2, 7-8, 15, and 17-26, and 29-37 are presented for examination.
2. This action is in response to the Amendment/Response and Affidavit on 10/5/09.

Applicant's Rule 132 Declaration has disqualified the primary reference of the prior office action.

In response, new grounds of rejections have been made in this non-final office action.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 21 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. As to claim 21, the limitation "wherein the jobs are reassigned based on the relative performances, by assigning jobs that benefited most from large complex cores to said large complex processor cores" is indefinite because it is unclear what the difference between the two sets of large complex cores, especially since the cores are claimed to be heterogeneous. Furthermore, the claimed limitation of "large complex cores" is a relative term which renders the claim indefinite. The term "large complex cores" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or

improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined claim(s) is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. “A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or anticipated by, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents).
6. **Claim 1 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 7,093,147 B2 in view of Kumar et al. (hereinafter Kumar) (“Processor Power Reduction Via Single-ISA Heterogeneous Multi-Core Architectures”, IEEE Computer Architecture Letters, Vol. 1, Issue 1, January 2002).**
7. As to claim 1, U.S. Patent No. 7,093,147 B2 teaches a computer system, comprising:

a plurality of computer processor cores in which at least two of the computer processor cores are heterogeneous, and wherein the plurality of computer processor cores all execute the same instruction set (col. 8, lines 50-53); and

a performance measurement (col. 8, lines 61-63) and transfer mechanism configured to move a plurality of computer processing jobs amongst the plurality of computer processor cores (col. 8, lines 64-67).

8. U.S. Patent No. 7,093,147 B2 is silent in matching requirements of the plurality of executing computer processing jobs to processing capabilities of the computer processor core.

9. However, Kumar teaches matching requirements of the plurality of executing computer processing jobs to processing capabilities of the computer processor core (Abstract). One of ordinary skill in the art would have known to modify U.S. Patent No. 7,093,147 B2 such that it would include the feature of matching requirements of the plurality of executing computer processing jobs to processing capabilities of the computer processor core, as taught in Kumar. The suggestion/motivation for doing so would have been to provide the predicted result of being able to dynamically choose the most appropriate core to meet specific performance and power requirements (see Abstract). Therefore, it would have been obvious to one of ordinary skill in the art to combine claim 1 of U.S. Patent No. 7,093,147 B2 and Kumar to obtain the invention of claim 1.

10. Claim 7 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 14 of U.S. Patent No. 7,093,147 B2 in view of Calder et al. (hereinafter Calder) (US 2004/0111708 A1).

11. As to claim 7, U.S. Patent No. 7,093,147 B2 teaches a method for operating multiple processor cores, comprising:

placing a plurality of computer processor cores on a single semiconductor die, in which at least two computer processor cores differ in processing performance, and in which all execute the same instruction set (col. 10, lines 39-46);

measuring the performance of each of a plurality of computer processing jobs hosted amongst the plurality of computer processor cores (col. 10, lines 49-51); and

transferring individual ones of said plurality of computer processing jobs amongst targeted ones of said plurality of computer processor cores to improve a throughput metric (col. 10, lines 52-55).

12. U.S. Patent No. 7,093,147 B2 is explicitly silent in obtaining a throughput metric that identifies throughput achieved by the computer processor cores as a function of workloads running on said computer processor cores.

13. However, Calder teaches a method for operating multiple processor cores, comprising: obtaining a throughput metric that identifies throughput achieved by a plurality of computer processor cores as a function of workloads running on said computer processor cores, wherein

the plurality of computer processor cores are on a single semiconductor die, in which at least two computer processor cores differ in processing capability, and wherein the computer processor cores execute the same instruction set; and transferring (switching) individual ones of a plurality of computer processing jobs amongst targeted ones of said plurality of computer processor cores to improve a throughput metric (single ISA architecture that has several heterogeneous cores) (lines 1-4 of [0049]; Abstract; claim 51).

14. One of ordinary skill in the art would have known to modify U.S. Patent No. 7,093,147 B2 such that it would include the feature of obtaining a throughput metric that identifies throughput achieved by the computer processor cores as a function of workloads running on said computer processor cores, as taught in Calder. The suggestion/motivation for doing so would have been to provide the predicted result of being able to dynamically choose the most appropriate core to meet specific performance and power requirements (see Abstract; [0049]). Therefore, it would have been obvious to one of ordinary skill in the art to combine claim 14 of U.S. Patent No. 7,093,147 B2 and Calder to obtain the invention of claim 7.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

15. Claims 1-2, 17, 19, 22, 32, and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Kumar et al. (hereinafter Kumar) (“Processor Power Reduction Via Single-ISA Heterogeneous Multi-Core Architectures”, IEEE Computer Architecture Letters, Vol. 1, Issue 1, January 2002).

16. Kumar (“Processor Power Reduction Via Single-ISA Heterogeneous Multi-Core Architectures”, IEEE Computer Architecture Letters, Vol. 1, Issue 1, January 2002) was cited in the previous office action on 6/26/09 as prior art made of record and not upon. This 102(b) date reference is now being relied upon in the rejection of this office action.

17. As to claim 1, Kumar teaches a computer system (computer system with Single-ISA Heterogeneous Multi-Core Architectures) (see Title and Abstract), comprising:

a plurality of computer processor cores in which at least two differ of the computer processor cores are heterogeneous, and wherein the plurality of computer processor cores execute the same instruction set (Single-ISA Heterogeneous Multi-Core Architecture) (see Title and Abstract); and

a performance measurement and transfer mechanism configured to move a plurality of executing computer processing jobs amongst the plurality of computer processor cores by matching requirements of the plurality of executing computer processing jobs to processing capabilities of the computer processor cores (evaluates the resource requirements of an application and chooses the core that can best meet these requirements) (see Title and Abstract).

18. As to claim 2, Kumar teaches further comprising: at least one of an operating system, hosted on the plurality of computer processor cores, firmware, and special-purpose hardware that includes the performance measurement and transfer mechanism, and the at least one of the operating system, firmware, and special-purpose hardware is configured to provide for a periodic test to determine relative performance of different jobs on different ones of the plurality of computer processor cores (see Abstract).

19. As to claim 17, Kumar teaches further comprising at least one of an operating system hosted on the plurality of computer processor cores, firmware, and special-purpose hardware that includes the performance measurement and transfer mechanism (see Abstract).

20. As to claim 19, Kumar teaches wherein the performance measurement and transfer mechanism is configured to transfer the executing computer processing jobs to a new assignment amongst the plurality of computer processor cores, collect performance statistics about execution at the new assignment, and then determine whether to reassign the executing computer processing jobs to different computer processor cores based on the performance statistics collected (see Title and Abstract).

21. As to claim 22, Kumar teaches wherein the determination of whether to reassign the jobs to different computer processor cores also is based on at least one of user-defined or workload-defined metrics (see Title and Abstract).
22. As to claim 32, Kumar teaches wherein the processing capabilities of the computer processor cores are defined by one or more of chip area, available resource, and relative speed of the computer processor cores (see Title and Abstract).
23. As to claim 34, Kumar teaches wherein the performance measurement and transfer mechanism is configured to further re-assign the plurality of executing computer processing jobs amongst the plurality of computer processor cores by repeatedly performing a test to match the requirements of the plurality of executing computer processing jobs to the processing capabilities of the computer processor cores (dynamically chooses the most appropriate core to meet specific performance/throughput and power requirements) (see Abstract).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

24. Claims 7-8, 15, 18, 24, 29-30, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar in view of Calder et al. (hereinafter Calder) (US 2004/0111708 A1).

25. As to claim 7, Kumar teaches a method for operating multiple processor cores, comprising:

obtaining a metric achieved by a plurality of computer processor cores as a function of workloads running on said computer processor cores, wherein the plurality of computer processor cores are on a single semiconductor die, in which at least two computer processor cores differ in processing capability, and wherein the computer processor cores execute the same instruction set (see Title and Abstract); and

transferring individual ones of a plurality of computer processing jobs amongst targeted ones of said plurality of computer processor cores (see Title and Abstract).

26. Kumar does not expressly teach the metric pertains to throughput and that the throughput metric is improved.

27. However, Calder teaches several heterogeneous cores having a single ISA architecture that tracks statistics to optimize run-time performance (lines 1-4 of [0049]; [0055]; claim 51). It would have been obvious to one of ordinary skill in the art to modify Kumar's multi-core processing system such that it would contain the feature of improving metrics of throughput, as taught and suggested in the multi-core processing system of Calder. The suggestion/motivation for doing so would have been to provide the predicted result of improving performance of the

system, specifically the run-time performance, for example (lines 1-4 of [0049]; [0055]; claim 51).

28. As to claim 8, Kumar teaches providing for a periodic test to determine relative performance of different jobs on different ones of the computer processor cores (see Abstract).

29. As to claim 15, Kumar (Abstract) and Calder ([0041]; Abstract) teaches further comprising: associating workloads for execution on specific processor cores based on annotations associated with the computer processing jobs. It would be obvious that the choosing of the most appropriate core to meet specific performance and power requirements would involve annotations for the matching because it annotations would provide the means for providing the information needed for the connection/matching of core to requirement.

30. As to claim 18, Kumar is silent in expressly teaching wherein the performance measurement and transfer mechanism is configured to maximize total system throughput. However, Calder teaches several heterogeneous cores having a single ISA architecture that tracks statistics to optimize run-time performance (lines 1-4 of [0049]; [0055]; claim 51). It would have been obvious to one of ordinary skill in the art to modify Kumar's multi-core processing system such that it would contain the feature of improving metrics of throughput, as taught and suggested in the multi-core processing system of Calder. The suggestion/motivation

for doing so would have been to provide the predicted result of improving performance of the system, specifically the run-time performance, for example (lines 1-4 of [0049]; [0055]; claim 51).

31. As to claim 24, Kumar does not expressly teach wherein movement of the executing computer processing jobs is constrained to occur only at operating system time slice intervals. However, Calder teaches wherein movement of the executing computer processing jobs is constrained to occur only at operating system time slice intervals ([0049]; 0053]; Abstract). It would have been obvious to one of ordinary skill in the art to modify Kumar's multi-core processing system such that it would contain the feature of wherein movement of the executing computer processing jobs is constrained to occur only at operating system time slice intervals, as taught and suggested in the multi-core processing system of Calder because it would allow for time-slicing scheduling, which is a known strategy for achieving the benefits of power-savings.

32. As to claim 29, Kumar teaches a method for operating multiple processor cores, comprising:

obtaining a metric that identifies throughput achieved by computer processor cores on a single semiconductor die as a function of workloads running on said computer processor cores (see Title and Abstract); and

assigning a plurality of computer processing jobs amongst a plurality of computer processor cores based on the throughput metric, wherein at least two of the computer processor

cores differ in size or complexity (cores of varying complexity) but execute the same instruction set (see Title and Abstract);

transferring the computer processing jobs to a new assignment amongst the plurality of computer processor cores (see Title and Abstract);

collecting statistics about execution performance of the computer processing jobs at the new assignment (performance and power statistics) (see Title and Abstract);

determining whether to reassign (choosing dynamically) the computer processing jobs to different computer processor cores based on the statistics collected (see Title and Abstract); and

utilizing relative performances of the computer processing jobs on different types of computer processor cores based on statistics collected (see Title and Abstract).

33. Kumar does not expressly teach the metric pertains to throughput and that the throughput metric is improved.

34. However, Calder teaches several heterogeneous cores having a single ISA architecture that tracks statistics to optimize run-time performance (lines 1-4 of [0049]; [0055]; claim 51). It would have been obvious to one of ordinary skill in the art to modify Kumar's multi-core processing system such that it would contain the feature of improving metrics of throughput, as taught and suggested in the multi-core processing system of Calder. The suggestion/motivation for doing so would have been to provide the predicted result of improving performance of the system, specifically the run-time performance, for example (lines 1-4 of [0049]; [0055]; claim 51).

35. In addition, Kumar in view of Calder does not explicitly teach building a data structure for the relative performances of jobs.

36. However, one of ordinary skill in the art would know that it is well known to use data structures to contain computing data. It would have been obvious to one of ordinary skill in the art to build a data structure for Kumar in view of Calder's recorded and tracked relative performances of core jobs so that the data can be organized and utilized for computer processing.

37. As to claim 30, Kumar teaches wherein the determination of whether to reassign the jobs to different computer processor cores also is based on at least one of user-defined or workload-defined metrics (see Title and Abstract).

38. As to claim 37, Calder teaches wherein the throughput metric indicates total system throughput, and wherein assigning maximizes the total system throughput, as indicated by the throughput metric ([0138]; [0055]; claim 51).

39. Claims 20-21 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar.

40. As to claim 20, Kumar teaches a computer system (computer system with Single-ISA Heterogeneous Multi-Core Architectures) (see Title and Abstract), comprising:

a plurality of computer processor cores in which at least two differ in processing performance, and wherein the plurality of computer processor cores execute the same instruction set (computer system with Single-ISA Heterogeneous Multi-Core Architectures) (see Title and Abstract); and

a performance measurement and transfer mechanism configured to move a plurality of executing computer processing jobs amongst the plurality of computer processor cores based on a measured throughput metric (matches the applications to the different cores based on a given performance/throughput requirement or goal) (see Title and Abstract),

wherein the performance and transfer mechanism is configured to swap execution (swaps when choosing most appropriate core during execution) of the executing computer processing jobs between the computer processor cores for a period of time (during execution, etc.), monitor resulting performance of relative performances of jobs on different types of computer processor cores (Abstract).

41. Kumar does not explicitly teach building a data structure for the relative performances of jobs. However, one of ordinary skill in the art would know that it is well known to use data structures to contain computing data. It would have been obvious to one of ordinary skill in the art to build a data structure for Kumar's tracked relative performances of core jobs so that the data can be organized and utilized for computer processing.

42. As to claim 21, Kumar teaches wherein the jobs are reassigned based on the relative performances, by assigning jobs that benefited most from large complex cores to said large complex cores (Abstract).

43. As to claim 33, Kumar teaches associating workloads for execution on specific processor cores based on annotations associated with the computer processing jobs (Abstract). It would be obvious that the choosing of the most appropriate core to meet specific performance and power requirements would involve annotations for the matching because it annotations would provide the means for providing the information needed for the connection/matching of core to requirement.

44. Claims 23 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar in view of Calder, and further in view of Nagae (US 6,006,248).

45. *Nagae was cited in the previous office action.*

46. As to claim 23, Kumar in view of Calder is silent in teaching wherein the performance/throughput metric comprises a number of instructions per second. However, Nagae teaches a job application distribution system among a plurality of processors, wherein CPU

performance is evaluated and may comprise of the number of instructions per second (col. 18, lines 35-43). One of ordinary skill in the art would have known to modify Kumar in view of Calder's performance/throughput metric such that it would comprise of the number of instructions per second because it would provide the predicted result of utilizing a standard and well-known unit that is common to the user.

47. As to claim 31, it is rejected for the same reasons as stated in the rejections of claims 23.

48. Claims 25-26 and 35-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar in view of Paker et al. (hereinafter Paker) ("A heterogeneous multi-core platform for low power signal processing in systems-on-chip", 2002).

49. As to claim 25, Kumar teaches a method for operating multiple processor cores, comprising:

assigning a plurality of computer processing jobs amongst a plurality of computer processor cores, wherein at least two of the computer processor cores differ in complexity (heterogeneous/different cores differ in complexity) but execute the same instruction set (see Title and Abstract), and

wherein assigning the plurality of computer processing jobs amongst the plurality of computer processor cores comprises matching requirements of the computer processing jobs to

processing capabilities of the computer processor cores based on the sizes or complexities of the computer processor cores (see Title and Abstract).

50. Kumar does not teach that its heterogeneous multi-core processor specifically refer to the cores differing in size.

51. However, Paker teaches a heterogeneous multi-core processing system such that cores differ in size and complexity so that the processing is both flexible and energy efficient (Abstract; last paragraph of page 73; first paragraph of page 74). Kumar and Paker are analogous art because they are in the same field of endeavor of multi-core processing and both are attempting to solve the same problem of improving processing performance. Thus, one of ordinary skill in the art would have known to modify Kumar's heterogeneous multi-core processing system such that it would include the feature of having its cores differ in size and complexity, as taught and suggested in Paker's heterogeneous multi-core processing system. The suggestion/motivation for doing so would have been to provide the predicted result of increased flexibility/customization through the differing cores, etc. (Paker - Abstract; last paragraph of page 73; first paragraph of page 74).

52. As to claim 26, Kumar teaches providing for a periodic test to determine relative performance of different jobs on different ones of the computer processor cores (see Abstract).

53. As to claim 35, Kumar teaches associating workloads for execution on specific processor cores based on annotations associated with the computer processing jobs (Abstract). It would be obvious that the choosing of the most appropriate core to meet specific performance and power

requirements would involve annotations for the matching because it annotations would provide the means for providing the information needed for the connection/matching of core to requirement.

54. As to claim 36, Kumar teaches repeatedly performing a test to match requirements of the computer processing jobs to the processing capabilities of the computer processor cores; and reassigning the plurality of computer processing jobs amongst the plurality of computer processor cores based on the repeated tests (dynamically chooses the most appropriate core to meet specific performance/throughput and power requirements) (see Abstract).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

55. Claims 1-2, 7-8, 15, 17-19, 22, 24, and 32-34 are rejected under 35 U.S.C. 102(a) as being anticipated by Calder et al. (hereinafter Calder) (US 2004/0111708 A1).

56. As to claim 1, Calder teaches a computer system (Abstract), comprising:

a plurality of computer processor cores in which at least two differ of the computer processor cores are heterogeneous, and wherein the plurality of computer processor cores execute the same instruction set (single ISA architecture that has several heterogeneous cores) (lines 1-4 of [0049]); and

a performance measurement and transfer mechanism configured to move (switching) a plurality of executing computer processing jobs amongst the plurality of computer processor cores by matching requirements of the plurality of executing computer processing jobs to processing capabilities of the computer processor cores ([0049]; Abstract).

57. As to claim 2, Calder teaches further comprising: at least one of an operating system, hosted on the plurality of computer processor cores, firmware, and special-purpose hardware that includes the performance measurement and transfer mechanism, and the at least one of the operating system, firmware, and special-purpose hardware is configured to provide for a periodic test to determine relative performance of different jobs on different ones of the plurality of computer processor cores (operating system) ([0108]; [0205]).

58. As to claim 7, Calder teaches a method for operating multiple processor cores, comprising:

obtaining a throughput metric that identifies throughput achieved by a plurality of computer processor cores as a function of workloads running on said computer processor cores,

wherein the plurality of computer processor cores are on a single semiconductor die, in which at least two computer processor cores differ in processing capability, and wherein the computer processor cores execute the same instruction set (single ISA architecture that has several heterogeneous cores) (lines 1-4 of [0049]; [0055]; claim 51); and

transferring (switching) individual ones of a plurality of computer processing jobs amongst targeted ones of said plurality of computer processor cores to improve a throughput metric ([0049]; see claim 51; Abstract).

59. As to claim 8, Calder teaches providing for a periodic test to determine relative performance of different jobs on different ones of the computer processor cores (lines 1-4 of [0049]; [0055]).

60. As to claim 15, Calder teaches further comprising: associating workloads for execution on specific processor cores based on annotations associated with the computer processing jobs ([0041]; Abstract).

61. As to claim 17, Calder teaches further comprising at least one of an operating system hosted on the plurality of computer processor cores, firmware, and special-purpose hardware that includes the performance measurement and transfer mechanism (operating system) ([0108]; [0205]).

62. As to claim 18, Calder teaches wherein the performance measurement and transfer mechanism is configured to maximize total system throughput ([0049]; see claim 51; Abstract).

63. As to claim 19, Calder teaches wherein the performance measurement and transfer mechanism is configured to transfer the executing computer processing jobs to a new assignment amongst the plurality of computer processor cores, collect performance statistics about execution at the new assignment, and then determine whether to reassign the executing computer processing jobs to different computer processor cores based on the performance statistics collected ([0049]; see claim 51; Abstract).

64. As to claim 22, Calder teaches wherein the determination of whether to reassign the jobs to different computer processor cores also is based on at least one of user-defined or workload-defined metrics ([0041]).

65. As to claim 24, Calder teaches wherein movement of the executing computer processing jobs is constrained to occur only at operating system time slice intervals ([0049]; 0053; Abstract).

66. As to claim 32, Calder teaches wherein the processing capabilities of the computer processor cores are defined by one or more of chip area, available resource, and relative speed of the computer processor cores ([0049]; [0055]).

67. As to claim 33, it is rejected for the same reasons as stated in the rejection of claim 15.

68. As to claim 34, Calder teaches wherein the performance measurement and transfer mechanism is configured to further re-assign the plurality of executing computer processing jobs amongst the plurality of computer processor cores by repeatedly performing a test to match the requirements of the plurality of executing computer processing jobs to the processing capabilities of the computer processor cores ([0049]; [0054]; [0055]; see claim 51; Abstract).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

69. Claims 20-21, 29-30, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Calder.

70. As to claim 20, Calder teaches a computer system (Abstract), comprising:

a plurality of computer processor cores in which at least two differ in processing performance, and wherein the plurality of computer processor cores execute the same instruction set (single ISA architecture that has several heterogeneous cores) (lines 1-4 of [0049]; [0055]); and

a performance measurement and transfer mechanism configured to move a plurality of executing computer processing jobs amongst the plurality of computer processor cores based on a measured throughput metric ([0049]; [0054]; [0055]; see claim 51; Abstract),

wherein the performance and transfer mechanism is configured to swap execution of the executing computer processing jobs between the computer processor cores for a period of time, monitor resulting performance (tracking statistics), and recording relative performances of jobs on different types of computer processor cores ([0049]; see claim 51; Abstract).

71. Calder does not explicitly teach building a data structure for the relative performances of jobs. However, one of ordinary skill in the art would know that it is well known to use data structures to contain computing data. It would have been obvious to one of ordinary skill in the art to build a data structure for Calder's recorded and tracked relative performances of core jobs so that the data can be organized and utilized for computer processing.

72. As to claim 21, Calder teaches wherein the jobs are reassigned based on the relative performances, by assigning jobs that benefited most from large complex cores to said large complex cores (lines 1-4 of [0049]; [0055]).

73. As to claim 29, Caldor teaches a method for operating multiple processor cores, comprising:

obtaining a throughput metric that identifies throughput achieved by computer processor cores on a single semiconductor die as a function of workloads running on said computer processor cores (single ISA architecture that has several heterogeneous cores) (lines 1-4 of [0049]; [0055]); and

74. assigning a plurality of computer processing jobs amongst a plurality of computer processor cores based on the throughput metric, wherein at least two of the computer processor cores differ in size or complexity (Being heterogeneous and different cores, Calder's cores differ in complexity) but execute the same instruction set (single ISA architecture that has several heterogeneous cores) (lines 1-4 of [0049]; [0055]);

transferring (switching) the computer processing jobs to a new assignment amongst the plurality of computer processor cores ([0049]; Abstract);

collecting statistics about execution performance of the computer processing jobs at the new assignment ([0049]; see claim 51; Abstract);

determining whether to reassign the computer processing jobs to different computer processor cores based on the statistics collected ([0049]; Abstract); and

75. Calder does not explicitly teach building a data structure for the relative performances of jobs. However, one of ordinary skill in the art would know that it is well known to use data structures to contain computing data. It would have been obvious to one of ordinary skill in the art to build a data structure for Calder's recorded and tracked relative performances of core jobs so that the data can be organized and utilized for computer processing.

76. As to claim 30, Calder teaches wherein the determination of whether to reassign the jobs to different computer processor cores also is based on at least one of user-defined or workload-defined metrics ([0041]).

77. As to claim 37, Calder teaches wherein the throughput metric indicates total system throughput, and wherein assigning maximizes the total system throughput, as indicated by the throughput metric ([0138]; [0055]; claim 51).

78. Claims 23 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Calder in view of Nagae (US 6,006,248).

79. As to claims 23 and 31, Calder is silent in teaching wherein the performance/throughput metric comprises a number of instructions per second. However, Nagae teaches a job application distribution system among a plurality of processors, wherein CPU performance is evaluated and

may comprise of the number of instructions per second (col. 18, lines 35-43). One of ordinary skill in the art would have known to modify Calder's performance/throughput metric such that it would comprise of the number of instructions per second because it would provide the predicted result of utilizing a standard and well-known unit that is common to the user.

80. Claims 25-26 and 35-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Calder in view of Paker et al. (hereinafter Paker) ("A heterogeneous multi-core platform for low power signal processing in systems-on-chip", 2002).

81. As to claim 25, Calder teaches a method for operating multiple processor cores (multi-core) ([0049]), comprising:

assigning a plurality of computer processing jobs amongst a plurality of computer processor cores, wherein at least two of the computer processor cores differ in complexity (heterogeneous multi-core) but execute the same instruction set (single ISA architecture that has several heterogeneous cores) (lines 1-4 of [0049]; [0055]), and

wherein assigning the plurality of computer processing jobs amongst the plurality of computer processor cores comprises matching requirements of the computer processing jobs to processing capabilities of the heterogeneous computer processor cores.

82. Being heterogeneous and different cores, Calder's cores differ in complexity.

83. Calder does not teach that its heterogeneous multi-core processor specifically refer to the cores differing in size.

84. However, Paker teaches a heterogeneous multi-core processing system such that cores differ in size and complexity so that the processing is both flexible and energy efficient (Abstract; last paragraph of page 73; first paragraph of page 74). Calder and Paker are analogous art because they are in the same field of endeavor of multi-core processing and both are attempting to solve the same problem of improving processing performance. Thus, one of ordinary skill in the art would have known to modify Calder's heterogeneous multi-core processing system such that it would include the feature of having its cores differ in size and complexity, as taught and suggested in Paker's heterogeneous multi-core processing system. The suggestion/motivation for doing so would have been to provide the predicted result of increased flexibility/customization through the differing cores, etc. (Abstract; last paragraph of page 73; first paragraph of page 74).

85. As to claim 26, Calder teaches providing for a periodic test to determine relative performance of different jobs on different ones of the computer processor cores (lines 1-4 of [0049]; [0055]).

86. As to claim 35, Calder teaches further comprising: associating workloads for execution on specific processor cores based on annotations associated with the computer processing jobs ([0041]; Abstract).

87. As to claim 36, Calder teaches repeatedly performing a test to match requirements of the computer processing jobs to the processing capabilities of the computer processor cores; and

reassigning the plurality of computer processing jobs amongst the plurality of computer processor cores based on the repeated tests ([0049]; [0054]; [0055]; see claim 51; Abstract).

Response to Arguments

88. Applicant's arguments have been fully considered but are now moot in view of the new grounds of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KENNETH TANG whose telephone number is (571)272-3772. The examiner can normally be reached on 8:30AM - 6:00PM, Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kenneth Tang/
Examiner, Art Unit 2195